Gigascale oriented Solid State flAsh Memory for EuRope

The project aims at the development of the technology for very high density Non Volatile Memories for mass storage applications down to the 2X nm technology node, addressing the field of portable multimedia applications.

At A Glance: GOSSAMER

Gigascale Oriented Solid State flAsh Memory for EuRope

Project Coordinator

Livio Baldi

Numonyx Italy S.r.l.

Tel: +39 039 6375015

Fax: +39 039 6375055

Email:livio.baldi@numonyx.com

Project website: www.fp7-gossamer.eu/

Partners:

Numonyx (ITA), Active Technologies (ITA), ASM Europe BV (NLD), IMEC (BEL), CNR-IMM-UOS MDM (ITA), Tyndall National Institute, University College Cork (IRL), IUNET (ITA), Fraunhofer CNT (DEU), University Braunschweig (DEU), ALMA Consulting Group (FRA), Jordan Valley (ISR), ASM Belgium NV (BEL), ASM Microchemistry Oy (FIN), NaMLab (DEU)

Qimonda (DEU) and University of Freiberg (DEU) in the first part of the project.

Duration: 1/2008 - 6/2011

Funding scheme: Large Scale Integrating Project

Total Cost: € 19,211,974

Main Objectives

During the last 15 years, ICTs has provided a number of radically new devices / techno-assistants that have improved the daily life of the EU citizen: mobile phone, digital camera, MP3 players, PC, PDA, credit cards, video on discs, flat screen, HD TV, fast communications (ADSL), car navigators, assisted driving, tablet PC, smart phones**….**

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The capability to provide continuously growing quantities of memory at ever decreasing costs has been the main success factor and one of the main contributors to the diffusion of the mobile information society. This constant progress has been possible through the technological evolution that has allowed a continuous scaling of the size of the memory cell, according to the so-called Moore's Law. NAND memories have become a serious contender to DRAM in production volumes and have replaced them as the main technology driver.

However physical limits are appearing to the continuation of this trend towards higher memory densities and they could mean an end, or a slowing down, for the progress of mobile electronics. **The GOSSAMER project aims at finding solutions to overcome these limits.**

The objectives of the project are:

- To develop a technology suitable for the realization of gigabyte Non Volatile Memory devices for mass storage, in the 3x and 2x technology nodes (x=2-8), based on charge-trapping NAND Flash architecture.
- To define material, cell architecture and processing technology.
- To realize a technology demonstrator with a memory size in the order of Gigabytes.

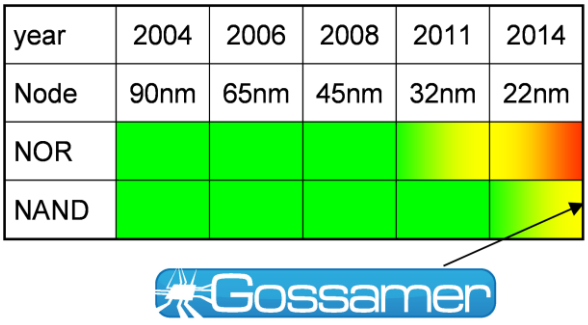
To this purpose a strong consortium has been put together, combining semiconductor manufacturers, suppliers of equipment and materials, Universities and Research Centers and with the participation of high-tech SME's.

Technical Approach

Target memory specifications, developed inside the **Management** Work Package will drive the activity of the two Work Packages: **WP1** - **Material Development** and **WP2 Cell Architecture**. Together with the process flow and critical process steps developed in **WP3 – Process Integration,** the results will flow into the design and realization of product-like demonstrators in **WP4**- **Demonstrator**, Characterization and reliability will be covered in Work Package 5 – **Characterization and Reliability**, while **WP6** – **Higher Density Architectures** will explore more risky approaches, like 3-D cell structures. **WP7** – **Training and Dissemination** will take care of the exploitation and dissemination of the results of the project.

Key Issues

At present NAND Flash technology is based on the floating gate architecture. In the deep submicron region physical limits are appearing mainly linked to cell to cell parasitic coupling and to the reduction of the stored charge. The project aims to investigate the possibility of replacing the conventional floating gate structure with a charge trapping layer.



Among the problems that need to be solved, we have to point out:

- Improvement of material properties of the stack toward a more efficient charge trapping capability;
- Development of materials with high dielectric constant for the blocking dielectric;
- Improvement of the charge trapping layer in terms of energy depth and density of traps
- Metal gate development to obtain a high work function.
- Optimization of the relative band-gap positions of the different layers composing the gate stack for the memory properties optimization
- In-depth understanding of the charge trapping and parasitic conduction mechanism in the new layers;
- Characterization and mitigation of the defect generation mechanisms during programming cycles.
- Asymmetric distribution of the charge during writing and erasing cycles, or in consequence of parasitic programming, which could lead to performance degradation.

Expected Impact

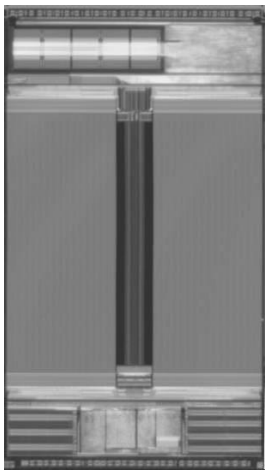
The expected impacts from the project are:

- Strengthened competitiveness of European *Nanoelectronics* through the involvement of European companies, including SME's along the complete value-chain.
- Enabling new electronics applications of socio-economic relevance such as:
  - data storage for portable communication systems and mobile electronics;
  - maps for navigation systems;
  - information storage for portable educational systems;
  - storage of medical records
  - data base for image recognition and biometric systems
- Giving to Universities access to advanced technology, and involving them in research activity that could have worldwide resonance.

Concrete Results

In the first years of the project material and cell architectures were developed leading to the characterization of functional mini-arrays.

In 2009 it was decided to anticipate a full industrial demonstrator, making use of the most advanced single exposure litho technology available.



A 1 Gbit NAND memory device was modified by Numonyx to become compatible with the new cell architecture. With the new architecture 1.8 Gcells could be accommodated in the same device area, even if only 1Gbit is addressable.

Fully functional samples have been obtained with good programming performances and acceptable reliability.